Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOEL PAGE, EDWIN DE ANGEL, WAI LAING LEE, LEI WANG, HONG ZHENG and CHUNG-KAI CHOW

Appeal No. 2001-2387
Application No. 09/153,864

ON BRIEF

Before KRASS, FLEMING, and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL AND ORDER

This is a decision on appeal from the Examiner's final rejection of claims 1-13. Claims 14-17 have been withdrawn from consideration as being drawn to a non-elected invention.

We reverse.

BACKGROUND

Appellants' invention is directed to a power on reset circuit which inhibits all clock signals that are used for digital logic operation until the applied voltage becomes stable.

Representative independent claim 1 is reproduced as follows:

1. A power on reset circuit, comprising:

a. a first circuit for applying a first voltage within said power on reset circuit, and

b. a circuit for starting phase locked loop when voltage applied by said first circuit exceeds a threshold, for inhibiting operation of at least a plurality of clocks until released, and for releasing all inhibited clocks once voltage stability is achieved.

Claims 1-13 stand rejected under the first paragraph of 35 U.S.C. § 112 for lack of an enabling disclosure.

Claims 1-13 stand rejected under the second paragraph of 35 U.S.C. § 112 as being indefinite.[1]

Rather than reiterate the viewpoints of the Examiner and Appellants regarding the rejections, we make reference to the answer (Paper No. 19, mailed May 22, 2001) for the Examiner's reasoning and to the appeal brief (Paper No. 18, filed March 5, 2001) for Appellants' arguments thereagainst.

OPINION

With regard to the rejection under the first paragraph of 35 U.S.C. § 112, the Examiner points out that box 795 in Figure 7 of the application does not include any specific structure of a

[1] The 35 U.S.C. § 102(b) rejection of claims 1, 6, 7 and 12 as being anticipated by Shaik, as stated in the final rejection (Paper No. 14, mailed September 29, 2000), has been withdrawn by the Examiner.

power on reset circuit to support the claimed functions (answer, page 3). The Examiner further argues that the relationship between the PLL and the plurality of clocks is not clear as circuit 795 is depicted in Figure 7 to be isolated from the rest of the circuitry (id.). Additionally, the Examiner questions the existence of the supporting structure for the recited "releasing all inhibited clocks once voltage stability is achieved" (answer, page 4).

Appellants argue that the required structural components such as power on circuits and threshold voltage detection circuits were known and readily available at the time of filing of the application (brief, page 6). Appellants, further rely on page 31, lines 32-35 of the specification and indicate that the POR circuit 795 of Figure 7 uses the specific protocol disclosed in page 32, lines 1-21 to ensure correct start up of the integrated circuit chip (brief, page 5). Additionally, Appellants refer to "TMI bus" in Figure 7 for providing an interconnection among POR circuit 795, switch converter 770 and clock control logic 725 and conclude that one of ordinary skill in the art could readily incorporate these known components to perform the recited functions (brief, pages 7 & 8).

The Examiner responds to Appellants' arguments by stating that the parts of the disclosure at pages 31 and 32, as referred to by Appellants, is directed toward the waveforms diagram shown in Figure 25 without disclosing how they are achieved (answer, page 5). The examiner further points out that power ON reset component 795 does not include component 725 whereas the recited claims appear to require some specific connections at least between a power ON reset circuit and a PLL (answer, page 6). Additionally, the Examiner questions the sufficiency of the disclosure for enabling one of ordinary skill in the art to connect the disclosed components such that the power ON circuit may have the ability to detect a threshold and a stable voltage and control different clock modes (answer, page 7).

We note that the first paragraph of 35 U.S.C. § 112 provides:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Our reviewing court has further stated that the enablement requirement is satisfied when the specification, when filed, enables one skilled in the particular art to use the invention

without undue experimentation. In re Wands, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988). Additionally, to be enabling, the specification must teach those of skill in the art "how to make and how to use the invention as broadly as it is claimed." In re Vaeck, 947 F.2d 488, 496, 20 USPQ2d 1438, 1445 (Fed. Cir. 1991).

We find that Appellants' specification contains various references to the power on reset circuit of Figure 7 applying the disclosed protocol that follows the timing diagram of Figure 25 such that different components are turned on or off at different times to ensure the operation of the clocks starts after the switch converter output stabilizes. The specification further indicates that when the supply voltage VDD is first applied, the power on reset circuit and the phase locked loop are activated and the duty cycle of the switch converter is set to unity (page 32, lines 4-12). After the switch converter is stabilized at 5.0 volts, the duty cycle hold is removed and the switch converter seeks its programmed value which is achieved after a settling time T_{SC_SETTLE}, after which the hold on all the clocks is removed and the chip starts to operate (page 32, lines 12-21). Therefore, to the extent that is claimed, the power on reset circuit provides the necessary controls for power on and the

control of the clock signals through the operation of the switch converter.

In view of the analysis above, we find that one skilled in the art would have been able to provide for the necessary connections for operating the power on reset circuit for inhibiting the clock signals until voltage stability is achieved according to the requirements of well known components without undue experimentation. We further find that the specification teaches the requirements for the proper connection of the power on reset circuit and the switch converter as broadly as defined by the scope of the claims. Accordingly, we reverse the rejection of claims 1-13 under the first paragraph of 35 U.S.C. § 112.

With respect to the rejection of claims under the second paragraph of 35 U.S.C. § 112, the examiner questions the clarity of the relationship between the first circuit and the circuit for starting a phase locked loop and how the clocks are inhibited and released (answer, page 4). Appellants argue that the claimed first circuit is directed to a power supply which applies a voltage to the power on reset circuit while such power supplies are known in the industry (brief, page 8). Appellants further point out that the terms "inhibit" and "release," as recited with

respect to the control of the clock circuits, is readily understood and do not need further detailed recitation in the broadest claims as to how the control is done (brief, pages 9 & 10).

In response, the Examiner indicates that the relationship between the components recited in claim 1 goes beyond the basic connection as the recited circuit apparently detects both a threshold voltage and a stable voltage and controls two different clock modes (answer, page 9). The Examiner further argues that it is not clear whether the power on reset circuit, as represented by box 795 in Figure 7, includes the first circuit or is a separate component (id.).

Analysis of 35 U.S.C. § 112, second paragraph, should begin with the determination of whether claims set out and circumscribe the particular area with a reasonable degree of precision and particularity; it is here where definiteness of the language must be analyzed, not in a vacuum, but always in light of teachings of the disclosure as it would be interpreted by one possessing ordinary skill in the art. In re Johnson, 558 F.2d 1008, 1015, 194 USPQ 187, 193 (CCPA 1977), citing In re Moore, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (1971). "The legal standard for definiteness is whether a claim reasonably apprises those of

skill in the art of its scope." In re Warmerdam, 33 F.3d 1354, 1361, 31 USPQ2d 1754, 1759 (Fed. Cir. 1994). Furthermore, our reviewing court points out that a claim which is of such breadth that it reads on subject matter disclosed in the prior art is rejected under 35 U.S.C. § 102 rather than under 35 U.S.C. § 112, second paragraph. See In re Hyatt, 708 F.2d 712, 715, 218 USPQ 195, 197 (Fed. Cir. 1983) citing In re Borkowski, 422 F.2d 904, 909, 164 USPQ 642, 645-46 (CCPA 1970).

Upon a careful review of the claim language and the specification, we find that the claimed "first circuit for applying a first voltage" clearly refers to a power supply. It is clear from the specification as a whole, and page 32 specifically, that a 5 volt VDD is first applied which activates the power on reset circuit and causes the phase locked loop to begin its oscillation. The specification on page 32 also provides for other components that perform the start up protocol applied by the power on reset circuit such as the switch converter for releasing the clocks after voltage stability is achieved. We further find that the details of the switch converter and the mode register for controlling the duty cycle of the switch converter and the recited releasing of the hold on the

inhibited clocks are also provided in the specification at pages 30-33.

In view of the above and in light of the specification as a whole, we find that the first circuit, the circuit for starting a phase locked loop and inhibiting/releasing the operation of the clock circuits are sufficiently defined and would reasonably apprise those skilled in the art of the scope of these limitations. Accordingly, we will not sustain the rejection of claims 1-13 under the second paragraph of 35 U.S.C. § 112.

CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1-13 under the first and the second paragraphs of 35 U.S.C. § 112 is reversed.

REVERSED

ERROL A. KRASS
Administrative Patent Judge

MICHAEL R. FLEMING
Administrative Patent Judge

MAHSHID D. SAADAT
Administrative Patent Judge

) BOARD OF PATENT APPEALS AND INTERFERENCES

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